

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111
Serial Number: 09/493,630
Filing Date: January 28, 2000
Title: VARIABLE DELAY LINE

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IN THE CLAIMS

Please delete claim 49.

1. (Original) A method of operation of a delay lock loop comprising:
comparing a phase of a first clock signal with a phase of a second clock signal to generate a first control signal;
delaying the first clock signal to generate a first delayed clock signal;
comparing a phase of the first delayed clock signal with the phase of the second clock signal to generate a second control signal; and
shifting a phase of the first clock signal in response to the first control signal and the second control signal.
2. (Original) The method of claim 1 wherein shifting comprises:
responsive to the first control signal, shifting the phase of the first clock signal by a first amount; and
responsive to the second control signal, shifting the phase of the first clock signal by a second amount, wherein the second amount is greater than the first amount.
3. (Original) The method of claim 1 further comprising:
delaying the second clock signal to generate a second delayed clock signal;
comparing a phase of the second delayed clock signal with the phase of the first clock signal; and
shifting the phase of the first clock signal a third amount in response to the third control signal.
4. (Original) The method of claim 3 wherein the third amount is substantially equal to the second amount.

5. (Original) A method of setting a delay value in a delay lock loop comprising:
delaying a first signal in a variable delay line to generate a second signal;
comparing a phase of the first signal with a phase of the second signal to generate a first control signal;
delaying the first signal by a first substantially fixed amount to generate a third signal;
comparing the phase of the second signal with a phase of the third signal to generate a second control signal;
responsive to the first control signal, adjusting the variable delay line by a first delay amount; and
responsive to the second control signal, adjusting the variable delay line by a second delay amount, the second delay amount being greater than the first delay amount.
6. (Original) The method of claim 5 further comprising:
delaying the second signal by a second substantially fixed amount to generate a fourth signal;
comparing the phase of the first signal with a phase of the fourth signal to generate a third control signal; and
responsive to the third control signal, adjusting the variable delay line by a third delay amount.
7. (Original) The method of claim 6 wherein the second delay amount and the third delay amount are substantially equal.
8. (Original) The method of claim 6 wherein the first substantially fixed amount and the second substantially fixed amount are substantially equal.
9. (Original) The method of claim 6 wherein the first delay amount and the second delay amount are opposite in polarity.

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10. (Original) A method of aligning the phase of a first signal external to a device and the phase of a second signal internal to the device comprising:
- receiving the first signal into the device, and subjecting the first signal to a device boundary delay to produce an internal first signal;
 - delaying the internal first signal in a variable delay line to generate the second signal, the variable delay line having a fine adjustment control and a coarse adjustment control;
 - delaying the second signal a substantially fixed amount to produce a delayed second signal;
 - comparing the internal first signal with the second signal, and responsive thereto, driving the fine adjustment control; and
 - comparing the internal first signal with the delayed second signal, and responsive thereto, driving the coarse adjustment control.
11. (Original) The method of claim 10 wherein prior to delaying the second signal or comparing the internal first signal with the second signal, the method further comprises subjecting the second signal to an additional delay substantially equal to the device boundary delay.
12. (Original) The method of claim 10 wherein the variable delay line has a second coarse adjustment control and the method further comprises:
- delaying the internal first signal the substantially fixed amount to produce a delayed internal first signal; and
 - comparing the delayed internal first signal and the second signal, and responsive thereto, driving the second coarse adjustment.
13. (Original) The method of claim 12 wherein the first coarse adjustment and the second coarse adjustment result in adjustments of opposite polarity.

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14. (Previously Presented) In a memory device having data output drivers configured to drive data signals external to the memory device, a method of aligning the data signals with an external clock signal comprising:
- receiving the external clock signal;
 - delaying the external clock signal in a variable delay line having a variable delay associated therewith, to produce an internal clock signal;
 - generating a first phase difference between the external clock signal and the internal clock signal;
 - comparing the first phase difference to a threshold;
 - when the first phase difference is above the threshold, changing the variable delay a first delay amount;
 - when the first phase difference is not above the threshold, changing the variable delay a second delay amount, the second delay amount being less than the first delay amount;
 - delaying the internal clock signal to produce a delayed internal clock signal;
 - generating a second phase difference between the external clock signal and the delayed internal clock signal;
 - changing the variable delay a third delay amount; and
 - driving a control input of the data output drivers with the internal clock.
15. (Original) The method of claim 14 wherein the data output drivers are sequential devices having clock inputs, and driving a control input comprises driving the clock inputs of the sequential devices.
16. (Original) The method of claim 14 wherein the data output drivers are devices having output enable inputs, and driving a control input comprises driving the output enable inputs of the data output drivers.

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17. (Previously Presented) The method of claim 14 wherein generating a second phase difference and comparing the second phase difference comprise:

delaying the internal clock signal by an amount substantially equal to the threshold to generate a delayed internal clock signal; and

comparing the delayed internal clock signal to the external clock signal.

18. (Previously Presented) In a memory device having data output drivers configured to drive data signals external to the memory device, a method of aligning the data signals with an external clock signal comprising:

receiving the external clock signal;

delaying the external clock signal in a variable delay line having a variable delay associated therewith, to produce an internal clock signal;

generating a phase difference between the external clock signal and the internal clock signal;

comparing the phase difference to a threshold;

when the phase difference is above the threshold, changing the variable delay a first delay amount;

when the phase difference is not above the threshold, changing the variable delay a second delay amount, the second delay amount being less than the first delay amount;

driving a control input of the data output drivers with the internal clock;

wherein generating a phase difference and comparing the phase difference comprise:

delaying the external clock signal by an amount substantially equal to the threshold to generate a delayed external clock signal; and

comparing the delayed external clock signal to the internal clock signal.

19. (Original) The method of claim 14 wherein the external clock signal has a period associated therewith, and the variable delay line delays the external clock signal such that the internal clock signal lags the external clock signal by an integer number of periods.

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20. (Previously Presented) In a delay line having a variable delay, a method of changing the variable delay comprising:

comparing a phase of a signal input to the delay line with a phase of a signal output from the delay line to produce a first phase difference;

when the first phase difference is larger than a first threshold, adjusting the variable delay by a first delay amount;

when the first phase difference is not larger than the first threshold and is larger than a second threshold, adjusting the variable delay by a second delay amount, the second delay amount being less than the first delay amount ;

delaying the signal input to the delay line to produce a third signal;

comparing the phase of the signal output from the delay line to the third signal to produce a second delay amount; and

adjusting the variable delay by a third delay amount .

21. (Original) The method of claim 20 further comprising:

responsive to the comparing, when the phase difference is smaller than the second threshold, holding the variable delay constant.

22. (Original) The method of claim 20 wherein the delay line comprises a plurality of delay elements, each of the plurality of delay elements having a unit delay, and wherein the second delay amount is substantially equal to one unit delay.

23. (Original) The method of claim 22 wherein the first delay amount is substantially equal to an integer number of unit delays.

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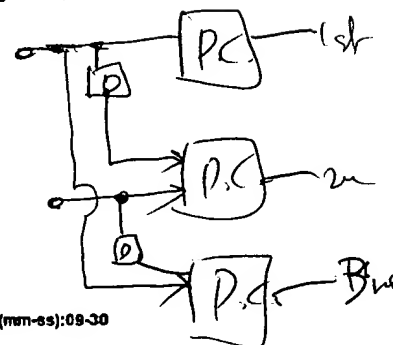
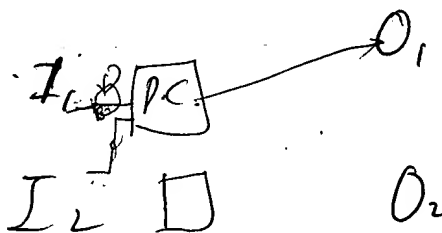
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24. (Currently Amended) A phase detector comprising:

- a first input node, a second input node, a first output node, and a second output node;
- a first phase comparator coupled to receive an external clock signal from between the first input node and coupled to receive an internal clock signal from [,] the second input node, and coupled to produce a fine adjustment signal on the first output node;
- a first ~~variable~~ delay line coupled to receive the external clock signal from the first input node and coupled to produce a delayed external clock signal; and
- a second phase comparator coupled to receive the delayed external clock signal from between the first delay line and coupled to receive the internal clock signal from [,] the second input node, and coupled to produce a course increase adjustment signal on the second output node;
- a second variable delay line coupled to receive the internal clock signal from the second input node and coupled to produce a delayed internal clock signal; and
- a third phase comparator coupled to receive the delayed internal clock signal from the second delay line and coupled to receive the external clock signal from the first input node, and coupled to produce a course decrease adjustment signal on the second output node .

25. (Previously Presented) A phase detector comprising:

- a first input node, a second input node, a first output node, and a second output node;
- a first phase comparator coupled between the first input node, the second input node, and the first output node;
- a first delay line coupled to the first input node;
- a second phase comparator coupled between the first delay line, the second input node, and the second output node;
- a third output node;
- a second delay line coupled to the second input node; and
- a third phase comparator coupled between the first input node, the second delay line, and the third output node.



26. (Currently Amended) A phase detector comprising:
- a first input node, a second input node, a first output node, and a second output node;
 - a first phase comparator coupled to receive clock signals from between the first input node and [,] the second input node, and for producing a fine increase adjustment signal on the first output node and for producing a fine decrease adjustment signal on the second output node;
 - a first delay line coupled to the first input node and coupled to produce a first delayed signal;
 - a second delay line coupled to the second input node and coupled to produce a second delayed signal;
 - a second phase comparator coupled to receive the first delayed signal from between the first delay line, coupled to the second input node, and the for producing a course increase adjustment signal on a third second output node; and
 - a third phase comparator coupled to receive the second delayed signal from the second delay line, coupled to the first input node, and the for producing a course decrease adjustment signal on a fourth output node.
- ~~wherein the first phase comparator is configured to produce at least one fine delay line adjustment control, and the second phase comparator is configured to produce at least one coarse delay line adjustment control.~~
27. (Previously Presented) A delay lock loop comprising:
- a variable delay line including a plurality of delay cells and an input connected to receive an external signal;
 - a shift register having a plurality of storage elements, each of the plurality of storage elements corresponding to one of the plurality of delay cells, the plurality of storage elements being arranged in a plurality of blocks of storage elements, the shift register having a fine control input node, and a coarse control input node;
 - a phase detector having a fine adjustment output node coupled to the fine control input node, and having a coarse adjustment output node coupled to the coarse control input node the phase detector further comprising:

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a first phase comparator operable for comparing a phase of the external signal to a phase of a variable delay signal output from the variable delay line and producing therefrom a first delay amount signal on the fine adjustment output node; and

a second phase comparator operable for comparing a phase of a delayed version of the external signal to the variable delay signal output from the variable delay line and producing therefrom a second delay amount signal on the coarse adjustment output node.

28. (Original) The delay lock loop of claim 27 wherein the shift register is configured to shift one of the plurality of storage elements in response to an asserted signal on the fine control input node.
29. (Original) The delay lock loop of claim 27 wherein the shift register is configured to shift one of the plurality of blocks of storage elements in response to an asserted signal on the coarse control input node, such that the variable delay line changes by more than one of the plurality of delay cells in response to the asserted signal.
30. (Original) The delay lock loop of claim 27 wherein the variable delay line includes an input node and an output node, and wherein the phase detector is configured to measure a phase difference between a signal on the input node of the variable delay line and a signal on the output node of the variable delay line.
31. (Original) The delay lock loop of claim 30 wherein the phase detector is configured to assert a coarse control signal on the coarse adjustment output node when the phase difference is above a threshold, and to assert a fine control signal on the fine adjustment output node when the phase difference is below the threshold.
32. (Original) The delay lock loop of claim 27 wherein the plurality of delay cells each exhibit substantially the same delay.

33. (Original) The delay lock loop of claim 27 wherein the plurality of delay cells do not all exhibit the same delay.

34. (Previously Presented) A variable delay line comprising:

a coarse adjustment portion comprising a first plurality of delay cells and a first shift register;

a fine adjustment portion comprising a second plurality of delay cells and a second shift register, wherein each of the first plurality of delay cells has a delay value larger than that of each of the second plurality of delay cells;

a first phase comparator operable for comparing a phase of an external clock signal to a phase of an internal clock signal output from the variable delay line and producing therefrom a first delay amount signal connected to control the fine adjustment portion; and

a second phase comparator operable for comparing a phase of a delayed version of the external clock signal and a phase of internal clock signal and producing therefrom a second delay amount signal connected to control the coarse adjustment portion.

35. (Previously Presented) The variable delay line of claim 34 wherein the first shift register is configured to be responsive to coarse adjustment signals from the second phase detector.

36. (Previously Presented) The variable delay line of claim 34 wherein the second shift register is configured to be responsive to fine adjustment signals from the first phase detector.

37. (Previously Presented) An integrated circuit comprising:

a variable delay line having an input node, an output node, a fine adjustment input node, and a coarse adjustment input node;

a first phase detector configured to compare a signal on the input node with a signal on the output node and drive signals onto the fine adjustment input node; and

a second phase detector configured to compare the signal on the output node with a delayed version of the signal on the input node and drive signals onto the coarse adjustment input node.

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33. (Original) The delay lock loop of claim 27 wherein the plurality of delay cells do not all exhibit the same delay.
34. (Previously Presented) A variable delay line comprising:
a coarse adjustment portion comprising a first plurality of delay cells and a first shift register;
a fine adjustment portion comprising a second plurality of delay cells and a second shift register, wherein each of the first plurality of delay cells has a delay value larger than that of each of the second plurality of delay cells;
a first phase comparator operable for comparing a phase of an external clock signal to a phase of a internal clock signal output from the variable delay line and producing therefrom a first delay amount signal connected to control the fine adjustment portion; and
a second phase comparator operable for comparing a phase of a delayed version of the external clock signal and a phase of internal clock signal and producing therefrom a second delay amount signal connected to control the coarse adjustment portion.
35. (Previously Presented) The variable delay line of claim 34 wherein the first shift register is configured to be responsive to coarse adjustment signals from the second phase detector.
36. (Previously Presented) The variable delay line of claim 34 wherein the second shift register is configured to be responsive to fine adjustment signals from the first phase detector.
37. (Previously Presented) An integrated circuit comprising:
a variable delay line having an input node, an output node, a fine adjustment input node, and a coarse adjustment input node;
a first phase detector configured to compare a signal on the input node with a signal on the output node and drive signals onto the fine adjustment input node; and
a second phase detector configured to compare the signal on the output node with a delayed version of the signal on the input node and drive signals onto the coarse adjustment input node.

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38. (Original) The integrated circuit of claim 37 wherein the fine adjustment input node comprises:
- a fine increase adjustment input node; and
 - a fine decrease adjustment input node.
39. (Original) The integrated circuit of claim 37 wherein the coarse adjustment input node comprises:
- a coarse increase adjustment input node; and
 - a coarse decrease adjustment input node.
40. (Original) The integrated circuit of claim 37 further comprising an output driver responsive to the signal on the output node of the variable delay line.
41. (Original) The integrated circuit of claim 37 wherein the output driver is a synchronous element having a clock input node, and the clock input node is coupled to the output node of the variable delay line.
42. (Original) The integrated circuit of claim 37 wherein the output driver includes an output enable input node coupled to the output node of the variable delay line.
43. (Original) The integrated circuit of claim 37 wherein the integrated circuit is a memory device.
44. (Original) The integrated circuit of claim 37 wherein the integrated circuit is an application specific integrated circuit.
45. (Original) The integrated circuit of claim 37 wherein the integrated circuit is a processor.

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46. (Previously Presented) A processing system comprising:
- a processor; and
 - a memory having a delay lock loop comprising:
 - a variable delay line including a plurality of delay cells and an input connected to receive an external signal;
 - a shift register having a plurality of storage elements, each of the plurality of storage elements corresponding to one of the plurality of delay cells, the plurality of storage elements being arranged in a plurality of blocks of storage elements, the shift register having a fine control input node, and a coarse control input node;
 - a phase detector having a fine adjustment output node coupled to the fine control input node, and having a coarse adjustment output node coupled to the coarse control input node the phase detector further comprising:
 - a first phase comparator operable for comparing a phase of the external signal to a phase of a variable delay signal output from the variable delay line and producing therefrom a first delay amount signal on the fine adjustment output node; and
 - a second phase comparator operable for comparing a phase of a delayed version of the external signal to the variable delay signal output from the variable delay line and producing therefrom a second delay amount signal on the coarse adjustment output node.
47. (Original) The processing system of claim 46 wherein the shift register is configured to shift one of the plurality of blocks of storage elements in response to an asserted signal on the coarse control input node, such that the variable delay line changes by more than one of the plurality of delay cells in response to the asserted signal.
48. (Original) The processing system of claim 46 wherein the variable delay line includes an input node and an output node, and wherein the phase detector is configured to measure a phase difference between a signal on the input node of the variable delay line and a signal on the output node of the variable delay line.

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49. (Deleted)

50. (Currently Amended) ~~The processing system of claim 49 wherein the phase detector further comprises:~~ A processing system comprising:

a processor; and

a memory having a delay lock loop that includes a phase detector comprising:

a first input node, a second input node, a first output node, and a second output node;

a first phase comparator coupled between the first input node, the second input node, and the first output node;

a first delay line coupled to the first input node; and

a second phase comparator coupled between the first delay line, the second input node, and the second output node;

a third output node;

a second delay line coupled to the second input node; and

a third phase comparator coupled between the first input node, the second delay line, and the third output node.

51. (Previously Presented) A processing system comprising:

a processor; and

a memory having a delay lock loop that includes a variable delay line comprising:

a coarse adjustment portion comprising a first plurality of delay cells and a first shift register;

a fine adjustment portion comprising a second plurality of delay cells and a second shift register, wherein each of the first plurality of delay cells has a delay value larger than that of each of the second plurality of delay cells;

a first phase comparator operable for comparing a phase of an external clock signal to a phase of a internal clock signal output from the variable delay line and producing therefrom a first delay amount signal connected to control the fine adjustment portion; and

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a second phase comparator operable for comparing a phase of a delayed version of the external clock signal and a phase of internal clock signal and producing therefrom a second delay amount signal connected to control the coarse adjustment portion.

52. (Original) The processing system of claim 51 wherein the first shift register is configured to be responsive to coarse adjustment signals from a phase detector.

53. (Original) The processing system of claim 52 wherein the second shift register is configured to be responsive to fine adjustment signals from a phase detector.